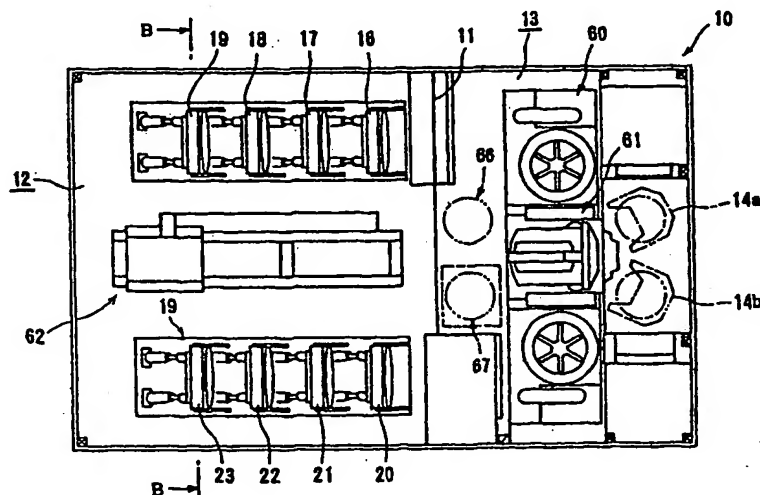


(51) 国際特許分類6 H01L 21/3205, 21/288, C23C 18/38	A1	(11) 国際公開番号 WO00/10200 (43) 国際公開日 2000年2月24日 (24.02.00)
(21) 国際出願番号 PCT/JP99/04349 (22) 国際出願日 1999年8月11日 (11.08.99) (30) 優先権データ 特願平10/239490 1998年8月11日 (11.08.98) 特願平11/30230 1999年2月8日 (08.02.99) 特願平11/220363 1999年8月3日 (03.08.99) (71) 出願人 (米国を除くすべての指定国について) 株式会社 荏原製作所 (EBARA CORPORATION) [JP/JP] 〒144-8510 東京都大田区羽田旭町11番1号 Tokyo, (JP) (72) 発明者; および (75) 発明者/出願人 (米国についてのみ) 本郷明久 (HONGO, Akihisa) [JP/JP] 小樽直明 (OGURE, Naoaki) [JP/JP] 井上裕章 (INOUE, Hiroaki) [JP/JP] 千代 敏 (SENDAI, Satoshi) [JP/JP] 池上徹真 (IKEGAMI, Tetsuma) [JP/JP] 三島浩二 (MISHIMA, Koji) [JP/JP] 奥山修一 (OKUYAMA, Shuichi) [JP/JP]	長井瑞樹 (NAGAI, Mizuki) [JP/JP] 〒144-8510 東京都大田区羽田旭町11番1号 株式会社 荏原製作所内 Tokyo, (JP) 君塚亮一 (KIMIZUKA, Ryoichi) [JP/JP] 〒156-0043 東京都世田谷区松原5丁目15番6号 Tokyo, (JP) 丸山恵美 (MARUYAMA, Megumi) [JP/JP] 〒226-0027 神奈川県横浜市緑区長津田7丁目1番43号 ガーデニアパーク 603 Kanagawa, (JP) (74) 代理人 渡邊 勇, 外 (WATANABE, Isamu et al.) 〒160-0023 東京都新宿区西新宿7丁目5番8号 GOWA西新宿4階 Tokyo, (JP) (81) 指定国 KR, US, 欧州特許 (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE) 添付公開書類 国際調査報告書	

(54) Title: WAFER PLATING METHOD AND APPARATUS

(54) 発明の名称 基板めっき方法及び装置



(57) Abstract

A method for plating through a simple manufacturing process a semiconductor wafer (W) so as to efficiently fill a fine recess (42) for interconnection made in the wafer (W) with a plating metal (43) having little voids and immune to contamination and to create an interconnection, comprising an electroless plating step of forming an initial film (41) on the wafer (W) and an electroplating step of filling the recess by electroplating using the initial film as the electricity feeding layer. An apparatus for plating a semiconductor wafer by such a method is also disclosed.

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/JP99/04349

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl⁶ H01L21/88, 21/288, C23C18/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl⁶ H01L21/88, 21/288, C23C18/38, C25D17/00-21/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-1999
 Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI [?ELECTROLYSIS+?ELECTROPLATING]

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 56-158424, A (Asahi Chemical Industry Co., Ltd.), 7 December, 1981 (07. 12. 81), Full text ; Fig. 1 (Family: none)	1, 8
X	JP, 7-193214, A (Mitsubishi Electric Corp.), 28 July, 1995 (28. 07. 95), Full text ; Figs. 1 to 9 & GB, 2285174, A & DE, 4446881, A	1
X	JP, 2-341, A (Seiko Epson Corp.), 5 January, 1990 (05. 01. 90), Full text ; Figs. 1 to 11 (Family: none)	1
Y	JP, 5-331653, A (NEC Corp.), 14 December, 1993 (14. 12. 93), Full text ; Figs. 1 to 13 (Family: none)	3, 6-7

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- *&* document member of the same patent family

Date of the actual completion of the international search
9 September, 1999 (09. 09. 99)

Date of mailing of the international search report
21 September, 1999 (21. 09. 99)

Name and mailing address of the ISA/
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